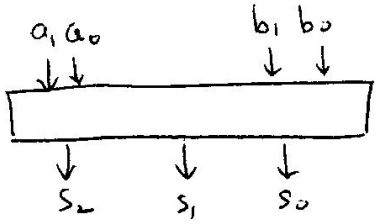
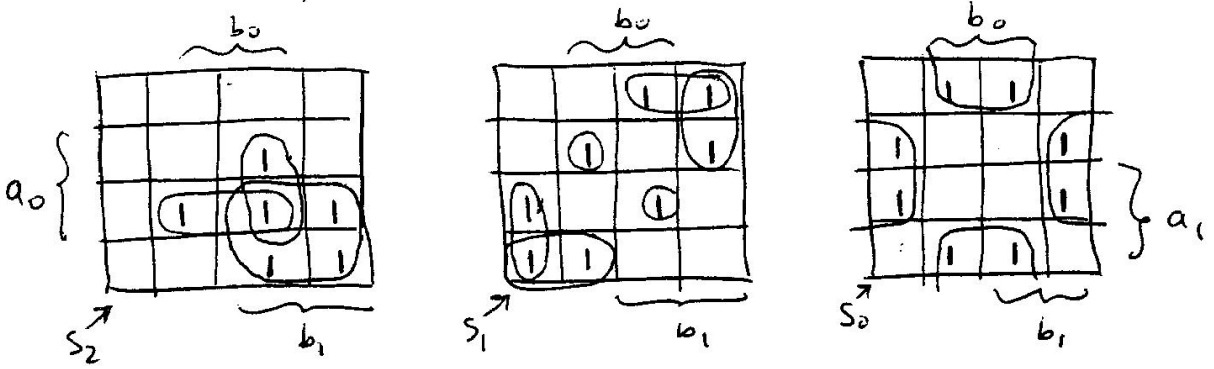
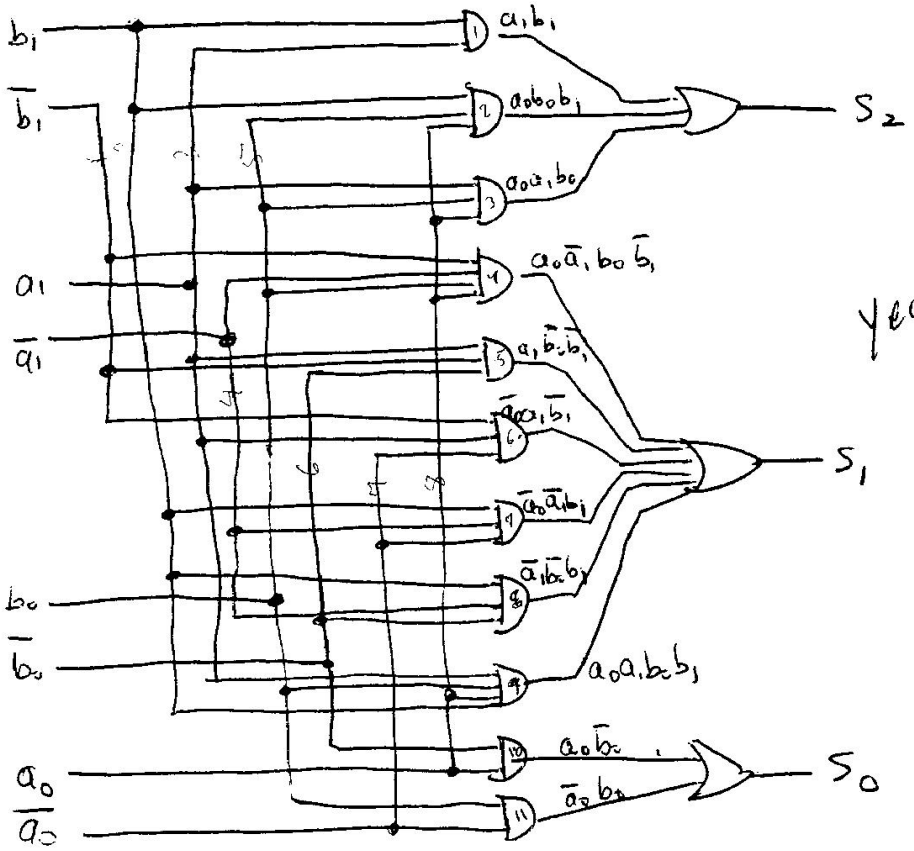
Example Problem 2-bit parallel adder (hard)



for example

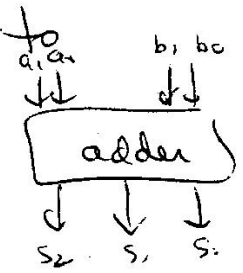
$a_1 a_0 = 10$
$b_1 b_0 = 11$
$= S_2 S_1 S_0 = 101$

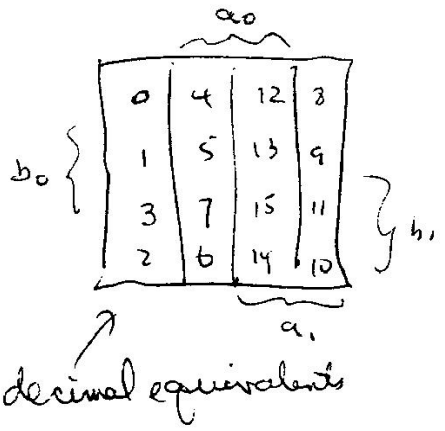




yech!

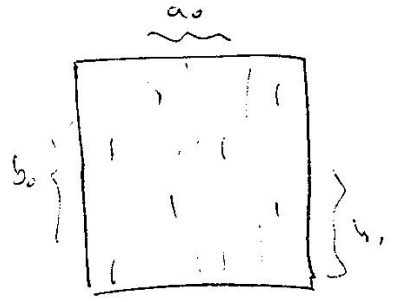
Now return to





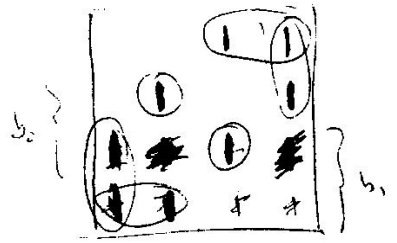
decimal equivalents

TT = BCD

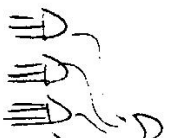


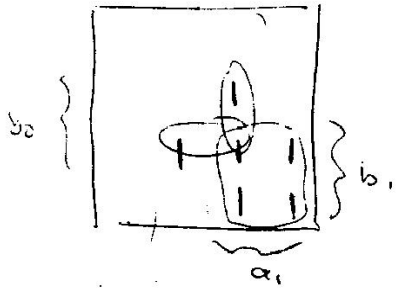
$S_0 = b_0 \oplus b_1 \oplus b_2 \oplus b_3$

↑ all odd numbers

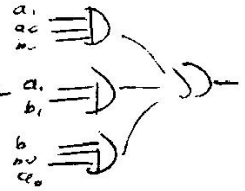


$S_1 =$





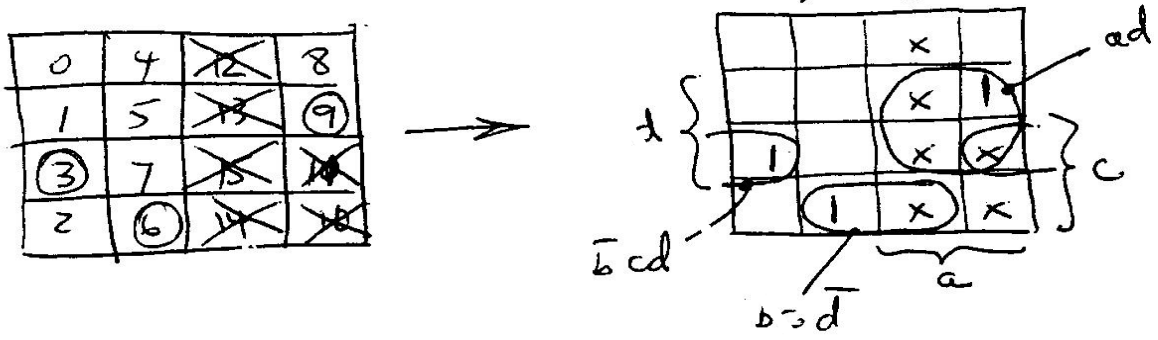
$S_2 =$

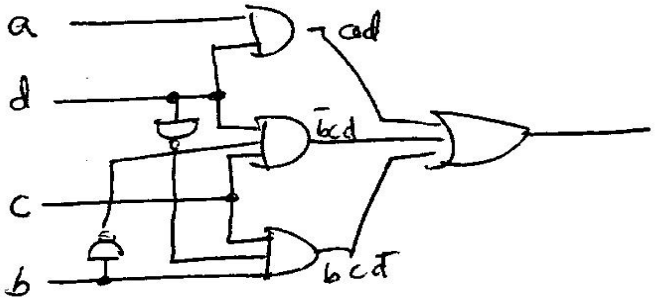


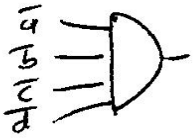
a1 a0	b1 b0	S2 S1
1 0	0 0	0 0
2 0 0	0 1	0 0
3 0 0	1 0	0 1
4 0 0	1 1	0 0
5 0 1	0 0	0 0
6 0 1	0 1	0 1
7 0 1	1 0	0 1
8 0 1	1 1	1 0
9 1 0	0 0	0 1
10 1 0	0 1	0 0
11 1 0	1 0	1 0
12 1 0	1 1	1 0
13 1 1	0 0	0 1
14 1 1	0 1	1 0
15 1 1	1 0	1 0
16 1 1	1 1	1 1

Example Problem with "don't cares"

Which BCD (binary coded decimal) integers are divisible by 3 ?
BCD means 4-bit code but 10-15 not allowed

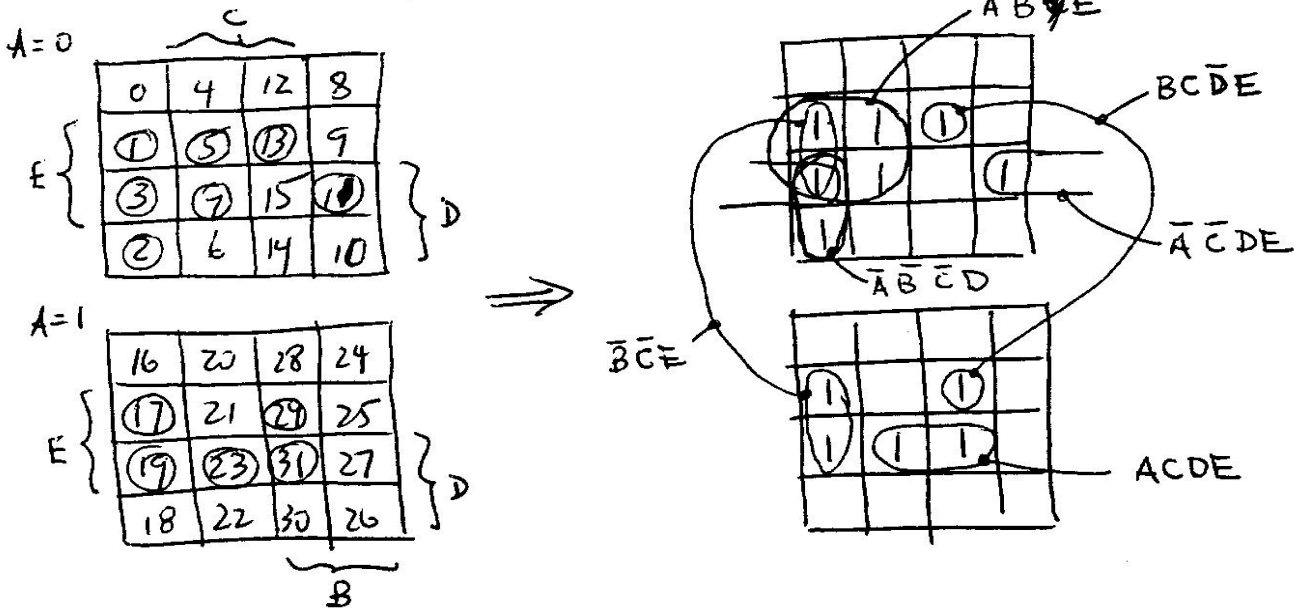


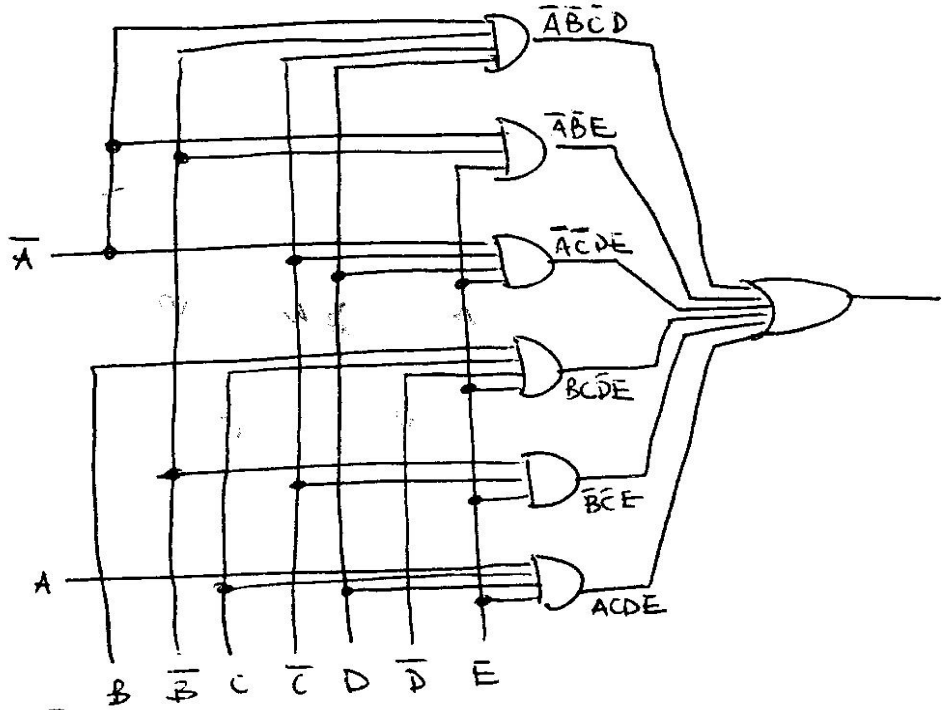


is 0 divisible by 3 ?
if so, need another AND gate: 

Example problem (very hard)

5-bit prime number detector



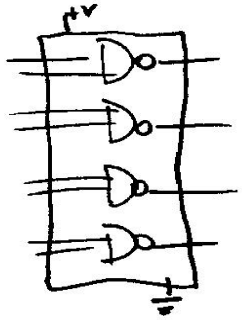


Digital Integrated Circuits

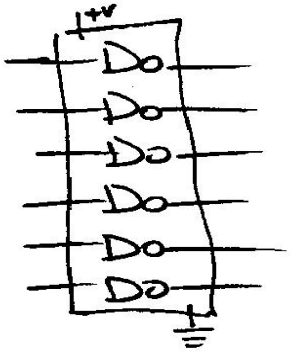
Small Scale Integration

Classical 7400 series TTL 14-pin DIPs

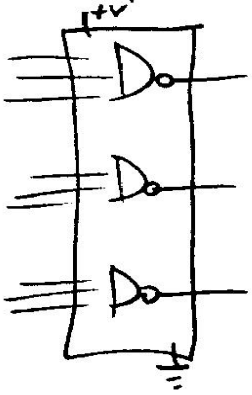
7400 Quad 2-input Nand



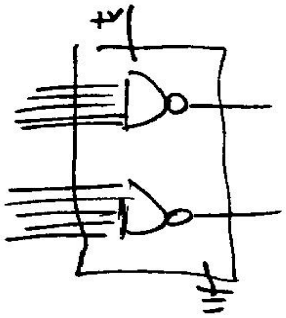
7404 Hex inverter



7410 Triple 3-input Nand



7420 Dual 4 (5) input Nand



If all chips cost the same: $C

1 2-input Nand costs $.25 C 1 4 input Nand costs $.5 C

Can measure effects of gate minimization